














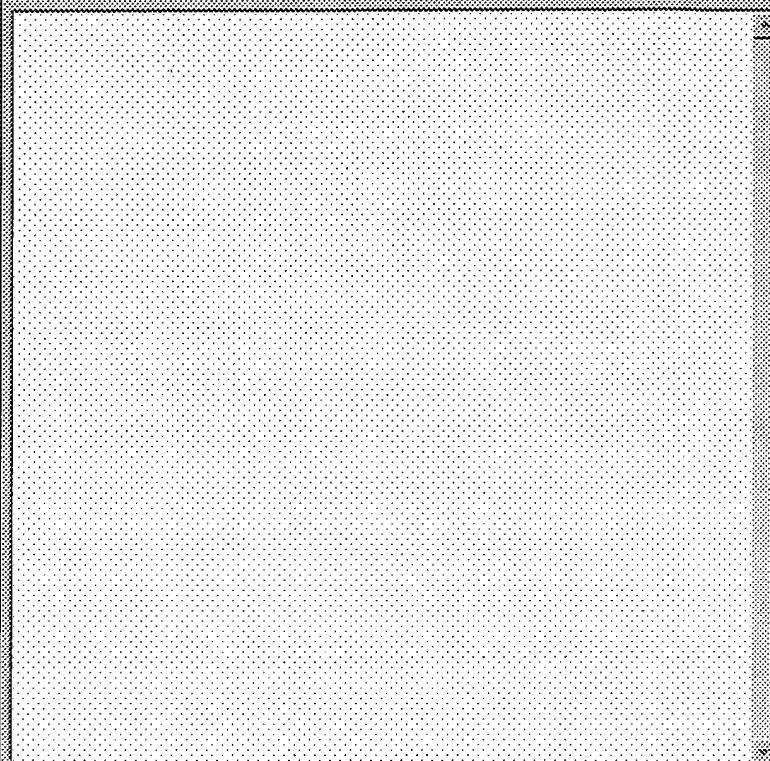
-  Drafts
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Figure 1. Schematic diagram of the experimental setup.

DB: US-AGPUB, LGPAT

[illegible]

☐ Highlight as for lesson tracks

[illegible]

	U	T	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif	Inventor
1	<input type="checkbox"/>	<input type="checkbox"/>	US 5990067 A	19990330	30	Multi-cluster parallel processing computer system	712/6	711/147; 711/150;		Zinguuzi, Sat
2	<input type="checkbox"/>	<input type="checkbox"/>	US 5892964 A	19990406	32	Computer bridge interfaces for accelerated graphics port and periph	712/33	710/1; 710/39;		Horan, Ron
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20030037224 A1	20030220	15	Computer system partitioning using data transfer routing mechanism	712/29	712/28		Oehler, Rich
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6611908 B2	20030826	20	Microprocessor architecture capable of supporting multiple heterogeneous	712/29	710/240; 710/317		Lentz, Derek
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5630166 A	19970513	9	Controlling requests for access to resources made by multiple processors	712/29	710/107; 710/240;		Gamache, S
6	<input type="checkbox"/>	<input type="checkbox"/>	US 4958273 A	19900918	19	Multiprocessor system architecture with high availability	712/29	710/113; 712/20;		Anderson, P
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6178493 B1	20010123	6	Multiprocessor stalled store detection	712/28	712/204; 712/29		Lentz, Peter S

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